

CLAIMS

What is claimed is:

1 1. A chipset comprising:
2 a graphics accelerator;
3 a memory controller; and
4 a queue mechanism including:

5 a first functional unit block (FUB) coupled to the graphics
6 accelerator; and
7 a second FUB coupled to the memory controller.

1 2. The chipset of claim 1 wherein the queue mechanism further comprises
2 control logic to facilitate an interface between the graphics accelerator and the
3 memory controller.

1 3. The chipset of claim 1 wherein the first FUB is operated based upon a
2 first clock domain and the second FUB is operated according to a second
3 clock domain.

1 4. The chipset of claim 1 wherein there is unidirectional signaling between
2 the first FUB and the second FUB, such that there will be a strobe and a
3 packet associated with the strobe that flows from the first FUB to the second
4 FUB.

1 5. The chipset of claim 3 wherein the second FUB comprises storage
2 elements in which to store information that is written into the queue
3 mechanism.

1 6. The chipset of claim 5 wherein the first FUB comprises:
2 logic associated with a load pointer, wherein the load pointer
3 indicates a location in the storage elements to store information; and
4 match logic.

1 7. The chipset of claim 6 wherein the second FUB comprises:
2 an unload pointer to indicate a location in the storage elements in
3 which information is to be read from; and
4 clock gating elements to gate the load pointer into the second clock
5 domain.

1 8. The chipset of claim 7 wherein the match logic compares the load and
2 unload pointer to determine whether information is stored in the queue.

1 9. The chipset of claim 8 wherein the load pointer is clock crossed to the
2 second clock domain in FUB 1 to save a clock of latency.

1 10. The chipset of claim 9 wherein the unload pointer is clock crossed to the
2 first clock domain in the second FUB.

1 11. The chipset of claim 10 wherein data to be stored in the storage elements
2 is directly flopped in the first clock domain within the second FUB.

1 12. The chipset of claim 10 wherein the clock crossed versions of the load
2 pointer and the unload pointer are used to determine at the second FUB if a
3 command is present.

1 13. The chipset of claim 12 wherein the availability of space in the storage
2 elements is determined at the match logic by using the load pointer and the clock
3 crossed version of the unload pointer.

1 14. A system comprising:
2 a first component;
3 a second component; and
4 a queue mechanism including:
5 a first functional unit block (FUB) coupled to the first component;
6 a second FUB coupled to the second component; and
7 control logic to facilitate an interface between the first component
8 and the second component.

1 15. The system of claim 14 wherein the first FUB is operated based upon a
2 first clock domain and the second FUB is operated according to a second

3 clock domain.

1 16. The system of claim 15 wherein the second FUB comprises storage
2 elements in which to store information that is written into the queue
3 mechanism.

1 17. The system of claim 16 wherein the first FUB comprises:
2 logic associated with a load pointer, wherein the load pointer
3 indicates a location in the storage elements to store information; and
4 match logic.

1 18. The system of claim 17 wherein the second FUB comprises:
2 an unload pointer to indicate a location in the storage elements in
3 which information is to be read from; and
4 clock gating elements to gate the load pointer into the second clock
5 domain.

1 19. A queue mechanism comprising:
2 a first functional unit block (FUB) coupled to a first component;
3 a second FUB coupled to a second component; and
4 control logic to facilitate an interface between the first component and the
5 second component.

1 20. The queue mechanism of claim 19 wherein the first FUB is operated

2 based upon a first clock domain and the second FUB is operated according to
3 a second clock domain.

1 21. The queue mechanism of claim 20 wherein the second FUB comprises
2 storage elements in which to store information that is written into the queue
3 mechanism.

1 22. The queue mechanism of claim 21 wherein the first FUB comprises:
2 logic associated with a load pointer, wherein the load pointer
3 indicates a location in the storage elements to store information; and
4 match logic.

1 23. The queue mechanism of claim 22 wherein the second FUB comprises:
2 an unload pointer to indicate a location in the storage elements in
3 which information is to be read from; and
4 clock gating elements to gate the load pointer into the second clock
5 domain.

1 24. The queue mechanism of claim 23 wherein the match logic compares the
2 load and unload pointer to determine whether information is stored in the
3 queue.

1 25. The queue mechanism of claim 24 wherein the load pointer is clock

2 crossed to the second clock domain in FUB 1 to save a clock of latency.

1 26. The queue mechanism of claim 25 wherein the unload pointer is clock
2 crossed to the first clock domain in the second FUB.

1 27. The queue mechanism of claim 26 wherein data to be stored in the storage
2 elements is directly flopped in the first clock domain within the second FUB.

1 28. The queue mechanism of claim 26 wherein the clock crossed versions of
2 the load pointer and the unload pointer are used to determine at the second FUB
3 if a command is present.

1 29. The chipset of claim 28 wherein the availability of space in the storage
2 elements is determined at the match logic by using the load pointer and the clock
3 crossed version of the unload pointer.

1 30. A computer system comprising:
2 a memory control hub (MCH) having:
3 a graphics accelerator;
4 a memory controller;
5 a queue mechanism including:
6 a first functional unit block (FUB) coupled to the graphics
7 accelerator; and

⁸ a second FUB coupled to the memory controller and

9 a main memory device coupled to the memory controller.

1 30. The computer system of claim 30 wherein the queue mechanism further
2 comprises control logic to facilitate an interface between the graphics accelerator
3 and the memory controller.

1 31. The computer system of claim 30 wherein the first FUB is operated based
2 upon a first clock domain and the second FUB is operated according to a
3 second clock domain.